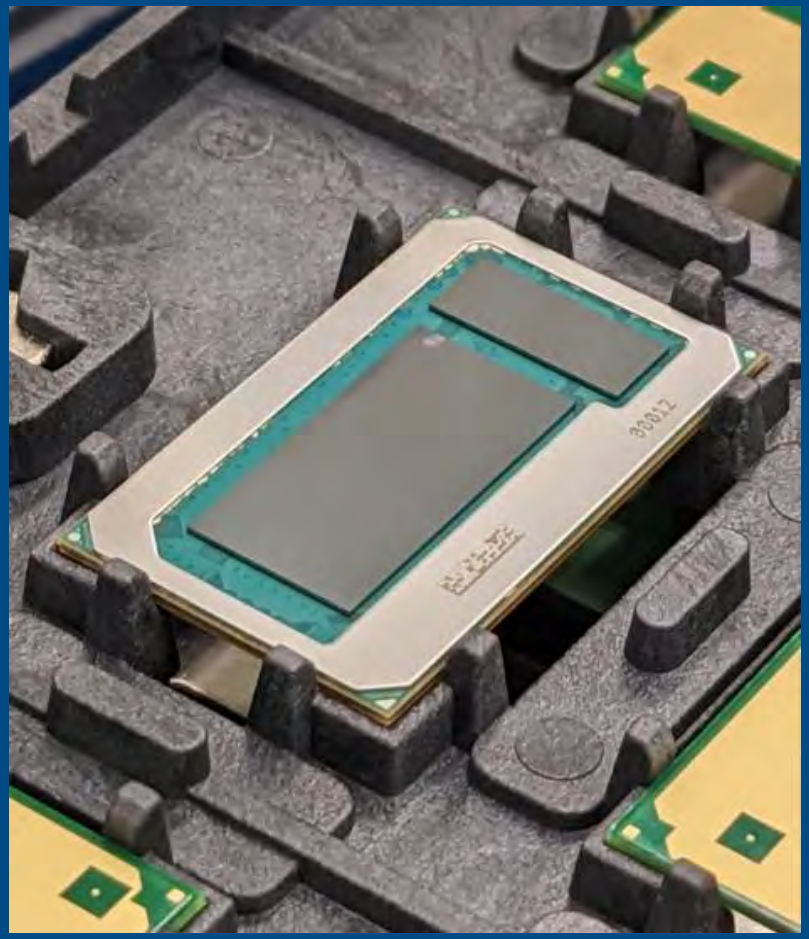
News Highlights

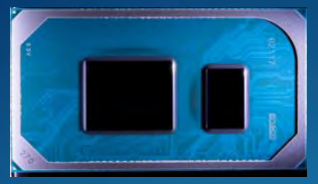
- Intel's breakthrough achievement enables continued scaling and advances Moore's Law – Glass substrates for advanced packaging coming later this decade.
- Glass substrates enable an order of magnitude improvement in design rules needed for future data center and AI products – Gains in performance and density over organic substrates.
- Chip architects can pack more "chiplets" in a smaller footprint on one package – Superior mechanical, physical and optical properties allow more transistors for better scaling and assembly of larger chiplet complexes.
- Improved density and performance properties will lead to lower overall cost and power usage – Chip architects will have greater flexibility in their designs.



Fully assembled glass substrate test chip

Intel Advanced Packaging Offerings

FCBGA / FCLGA

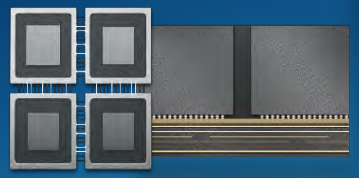


bump pitch ~**100µm**

- Leading global user/assembler of FCBGA (>40% share)
- Support to 120x120mm
- Enabled STIM w/BGA
- Multi-ball BGA for managing warpage
- PoINT architecture for cost savings

2D/MCP

Embedded Multi-die Interconnect (EMIB)

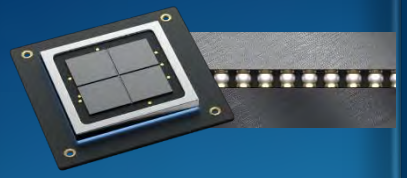


bump pitch **55→45 →45/36µm w/TSV**

- Products shipping since 2017
- High Bandwidth
- Supports large form factor: 4.5x reticle equiv→6x+ reticle equiv.

2.5D

Foveros

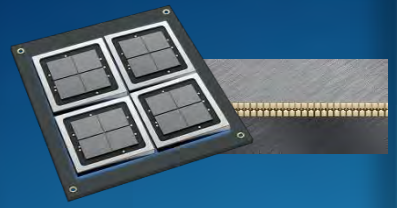


bump pitch **36→25µm**

- First product in 2019, HVM ramp from 2023
- Wafer-level packaging plus silicon interposer capability
- Optimized for cost/performance

2.5D/3D

Foveros Direct



bump pitch **< 10µm**

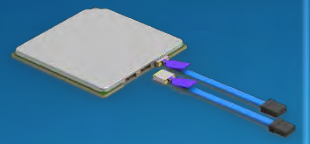
- Direct Cu to Cu bonding for high density and low resistance interconnects
- Best power per bit performance (~0.05pJ/bit)

3D Hybrid Bonding

Glass Core Substrate

- Continued feature scaling
- Improved power delivery
- Enables 448G / HSIO

Co Packaged Optics



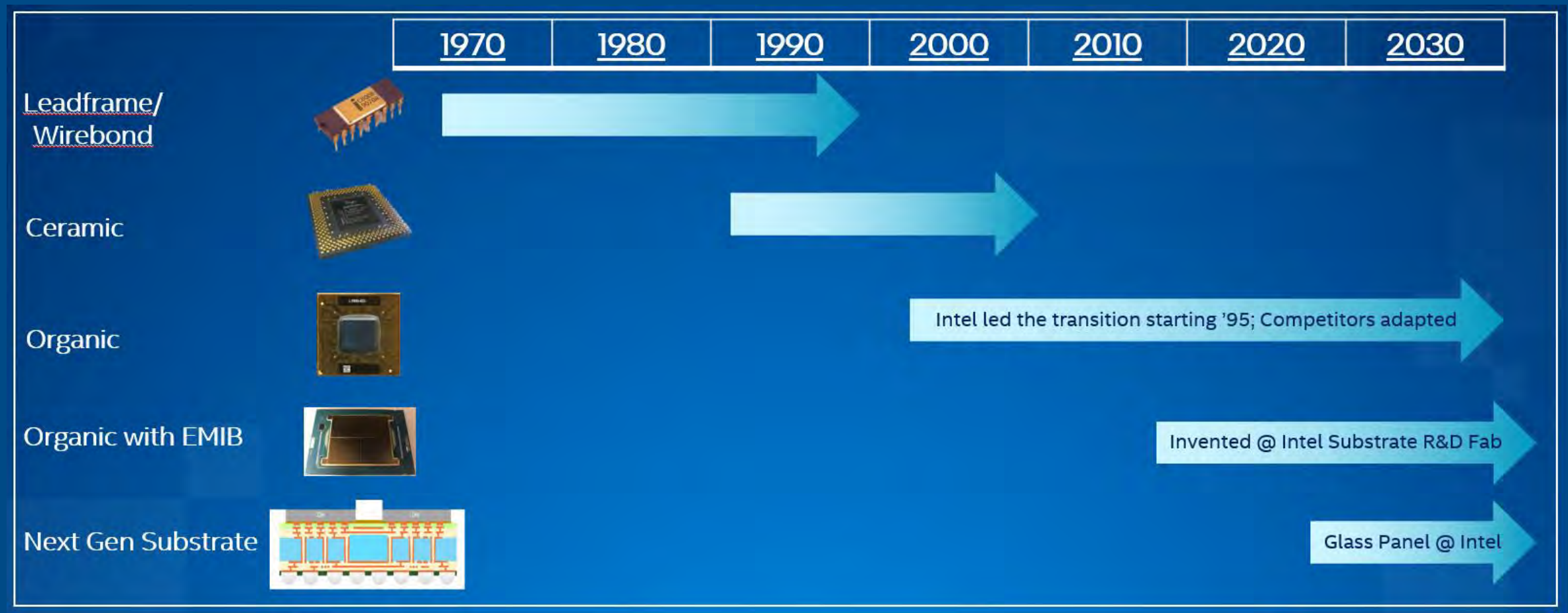
- Pluggable connector
- Glass-based coupling with integrated Waveguides
- Enables high yield, low cost flow

Next Gen Interconnects

*Source: Intel internal analysis, Prismark, TechSearch (2023)

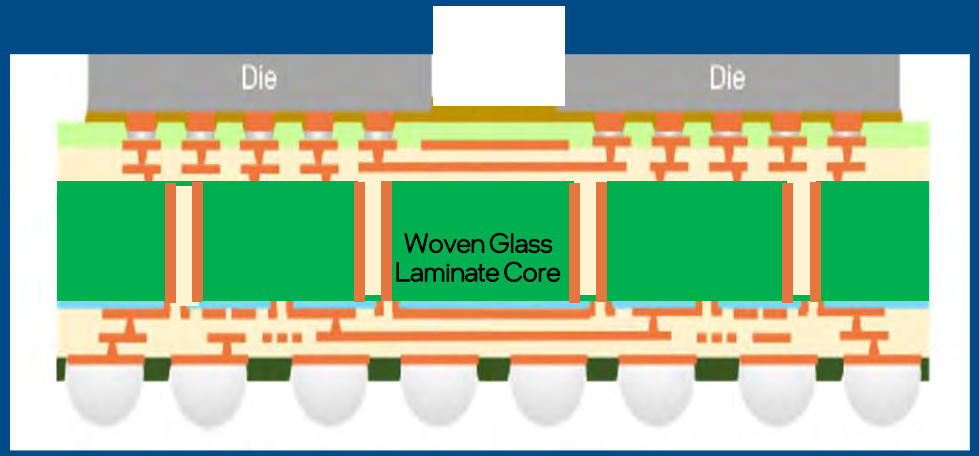
Processor Substrate History

- Major substrate technology shifts every ~15 years.
- Transition from organic to glass will occur in this decade.
- Organic and glass substrates will co-exist.



Motivation for Glass Core Substrates

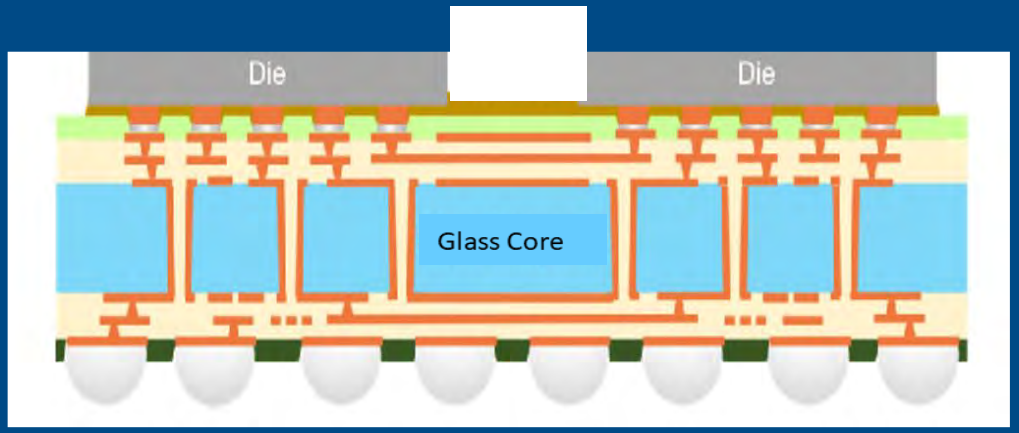
Organic Substrate



Organic substrates leverage traditional PCB-like cores with woven glass laminates

- Provides a low cost, easily manufacturable material set with off the shelf laminates available from leading suppliers

Glass Core Substrate



Glass core substrate enable significant improvement to both electrical and mechanical properties

- Tunable Modulus and CTE closer to silicon → Large form factor enabling
- Dimensional stability → Improved feature scaling
- High (~10x) through-hole density → improved routing and signaling
- Low Loss → High speed signaling
- Higher Temperature capability → Advanced Integrated Power Delivery

Glass Core has similar properties as Si → Dimensional stability and ability to scale

*Based on internal analysis of Intel products and projections of future Intel products

Glass Core Benefits

		Scaling Enabled by Glass Core	Product Value
1	Feature Scaling	<5/5um Line/Space & <100um TGV* pitch	Reduce metal layer count and/or package size OR add more function/cores
2	Bump Pitch Scaling	Enables D2D bump pitch <36u on substrate and core bump pitch <80um	Reduced die area/power and increased interconnect density
3	More SI Content / Larger Package Size	Enables 50% larger die complex area in same package, >8x reticle Si and package size up to 240x240 mm	Enables scaling of die area complex and package size in HPC
4	High Speed I/O	Smooth Cu + Ultra-low loss dielectric + TGV pitch	Scaling to 448G without the complexity and cost of transitioning to optical**
5	Power Delivery	Advanced IPD	Improved Performance

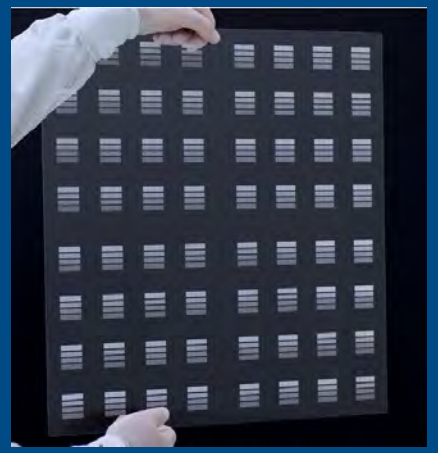
*Through Glass Via

** With Organic Substrate

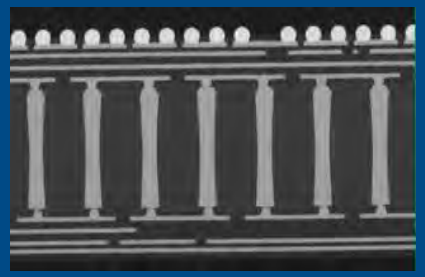
*Based on internal analysis of Intel products and projections of future Intel products

Intel Product Update

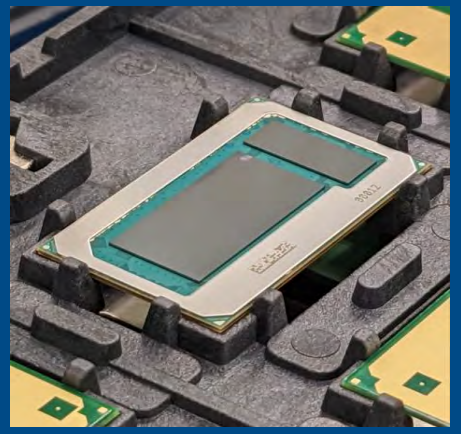
- Intel work on glass goes back a decade
- Fully integrated glass R&D line with over $1B investment in Chandler, AZ
- Close work with equipment and materials partners to enable ecosystem
- Electrically functional assembled MCP test vehicle with 3 layers of RDL and TGV of 75um
- Filled through glass vias with ~20:1 aspect ratio for 1mm core thickness suited for AI and Data Center
- Over 600 inventions related to architecture, process, equipment and materials



Glass Panel with Through Glass Vias (TGV)



X-section of a substrate test vehicle with 3 RDLs and 75um TGVs for client products



Fully assembled glass substrate

*Intel Images

Why Glass vs. Organic? (New details not shared in May)

- Tolerance for higher temperatures offers 50% less pattern distortion.
- Glass substrates have ultra-low flatness for improved depth of focus for lithography.
- Dimensional stability needed for extremely tight layer to layer interconnect overlay.
- Up to 10x increase in interconnect density possible with glass.
- Improved mechanical properties of glass enable ultra-large form-factor packages with very high assembly yields.
- Glass provides improved flexibility in setting design rules for power delivery and signal routing.
- Ability to seamlessly integrate optical interconnects, as well as embed inductors and capacitors into the glass at higher temperature processing.
- Better power delivery solutions while achieving high-speed signaling that is needed at much lower power.