ALC4080
(PN: ALC4080-VA2-CG)

7.1+2 CHANNEL HIGH FIDELITY USB AUDIO CODEC

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC4080 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2020/07/22	First release.
1.1	2020/08/18	Modify mass production :A2 Version

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1. General Description

The ALC4080 is a single-chip multi-channel USB audio codec that embeds a USB 2.0 controller with a high performance audio codec. For USB audio function, it supports a standard USB audio device with HID class designed for PC Motherboard and multi-channel audio system/device in all major commercial operating systems, e.g., Windows, Linux, iOS, macOS, and Android.

The ALC4080 provides ten DAC channels that simultaneously support 7.1-channel playback, plus 2 channels of independent stereo output (multiple streaming) through the front panel stereo output with up to 120dB Signal-to-Noise (SNR) for PCM stream playback. The ALC4080 also provides a Direct-Stream-Digital (DSD) decoder to help users enjoy high quality DSD stream content and create their own DSD stream with minimum quality loss caused by DA converters. Three stereo ADCs are integrated and can support multiple analog audio inputs, including a 110dB SNR stereo line level input and microphone array with software features Acoustic Echo Cancellation (AEC), Beam Forming (BF), Noise Suppression (NS) and Far Field voice Pick up (FFP) technologies.

All analog I/O are input and output capable, and all can be re-tasked according to user definitions. There are three headphone amplifiers integrated at analog output ports (port-D/port-E/port-F). The headphone amplifier at port-D (FRONT) is a cap-free type that can save an external coupling capacitor and provide less distortion and less pop affects. This port-D headphone amplifier has 2 Vrms output capability and can drive high impedance (up to 600Ω) headphones; then with impedance sensing function for auto-adjusting the output volume with the excellent audio response preferred by musicians and game players.

Support for 16/20/24-bit SPDIF output with up to 192kHz sample rate offers easy connection of PCs to High Definition Media Interface (HDMI) transmitters or consumer electronic products such as digital decoders and A/V receivers.

ALC4080 is USB 2.0 standard high-speed, high performance audio codec for USB Type-C multi-channel (Ture 7.1 channel) Gaming headphone/headset and audio adaptor applications. With software utilities such as environment sound emulation, multiple-band and independent software equalizer, dynamic range compressor and expander, optional third party software features from Dolby, DTS, Waves and Fortemedia, and Creative Host Audio, the ALC4080 offers the highest sound quality, providing an excellent entertainment package and game experience for PC users.

2. Features

2.1. Hardware Features

2.1.1. USB Controller Features

- Compliant with USB Specification 2.0 Full-Speed and High-Speed transfer mode
- Compliant with USB Audio Class Specification Rev1.0 and 2.0 and ADC3.0
- Compliant with USB HID 1.11 Device Class Specification
- Compliant with USB DFU/ Microsoft CFU Class Specification for Firmware update
- Supports one isochronous endpoint used for 2~8 channel playback streaming
- Supports three isochronous endpoints used for 2 channel playback streaming
- Supports three isochronous endpoints used for 2 channel recording streaming
- Supports one endpoint0 for control transfer and two endpoints for interrupt transfer
- Supports Selective Suspend mode
- Supports USB LPM (Link Power Management)-L1 protocol for power saving
- Supports jack detection and GPIOs remote wakeup function in suspend mode
- Internal clock generation supports non-crystal design

2.1.2. Micro Controller Unit

- On-chip high-performance and low-power MCU
- Ultra-low power consumption when MCU is at idle state
- MCU controls connection to USB bus for re-enumeration without hot-plug
- Internal programmable memory support for customized audio function
- Watchdog control for MCU reset and interrupt
- Configurable VID (Vendor ID), PID (Product ID), and serial number string

2.1.3. Audio Functions

- Front DAC(DAC02) to Port-D with 120dB SNR (A-weighting)
- Front DAC(DAC02) to Port-E with 110dB SNR (A-weighting)
- Port-C and Port-F to main ADC(ADC09) with 110dB SNR (A-weighting)
- DACs (except Front DAC) with >95dB SNR (A-weighting), ADCs with >92dB SNR (A-weighting)
- Ten DAC channels support 16/24/32-bit PCM for 7.1 channel sound playback, plus 2 channels of concurrent independent stereo sound output (multiple streaming) through the front panel output
- Three stereo ADCs support 16/24-bit PCM format, multiple stereo recording
- All DACs supports 44.1k/48k/88.2k/96k/176.4k/192k/384kHz sample rate
- All ADCs supports 44.1k/48k/88.2k/96k/176.4k/192kHz sample rate
- SPDIF-OUT supports 16/24-bit and 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- Supports two independent 2-channel hardware native DSD decoder (64Fs and 128Fs) and DoP decoder (64Fs) to Port-D and Port-E
- 0.75dB per step output volume and input volume control
- All analog jacks (Port-A to Port-H, except Port-D) are stereo input and output re-tasking
- Port-D/E/F built-in headphone amplifiers, Port-D headphone amplifier is cap-free type and has 2 Vrms output capability
- Supports Headphone impedance sensing (Port-D cap-free headphone amplifier)
- Port-B/C/E/F with software selectable boost gain (+10/+20/+30dB) for analog microphone input
- Analog microphone bias voltages (VREFOUT) are software selectable (2.25V/3.2V/4.0V)
- External PCBEEP input detect and internal BEEP generator is integrated
- Supports four jack detection pins, each designed to detect up to 2 jacks
- Two digital microphone interfaces sharing one digital microphone clock
- 4 GPIOs (General Purpose Input and Output) for customized applications. All GPIO are pin shared with SPDIF-OUT, digital MIC, and PWM signal.
- SPDIF-OUT supports 16/20/24-bit format and 44.1/48/88.2/96/192KHz sample rate

- Supports LED control according to music tempo/rhythm (beat mode), and pumping signal (PWM) in standby mode
- Supports impedance sensing for headphone device
- Supports Boot-up Logo and key buttons sound-out by firmware code
- Built-in analog LDOs for converters, mixer, and headphone amplifiers

2.1.4. Miscellaneous

- Supports hardware CRC32, ECDSA and SHA256 for firmware security
- Multi GPIOs for customized applications (pin-shared with digital microphone interface and other digital functions)
- I2C control interface; supports master/slave mode
- Toggle PWM LED driver and controller upon firmware or custom driver customizations
- Front DAC (DAC02) supports rhythm detect LED Beat mode
- 48-pin QFN 6mm x 6mm 'Green' package

2.2. Software Features

- USB Audio Class compliant; operates with native driver in Microsoft Windows, Linux, Android, iOS, and macOS
- Realtek custom audio driver provides a certified logo driver for Microsoft Windows System
- Meets Microsoft WLP audio performance requirements and WHQL certification
- Realtek Control Panel (Realtek Audio Manager) for enhanced user experience:
  - Audio I/O Jack and Device settings and controls
  - Application Enhancements for both voice processing and audio post processing and effects
  - Reduces audio software development and usage complexity
- Selective suspend function saves power in Standby mode
- WaveRT-based audio function driver for Windows OS
- Direct Sound 3D™ compatible
- I3DL2 compatible

- 7.1+2 channel multi-streaming enables concurrent gaming/VoIP
- Emulation of 26 sound environments to enhance gaming experience
- Multiband software equalizer and tools provided
- Voice Cancellation and Key Shifting effect
- Dynamic range control (expander, compressor, and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), Beam Forming (BF), Far Field Voice Pick up (FFP) technologies for voice applications
- Smart multiple streaming operation

3. System Applications

- Desktop multimedia PCs
- USB docking station with audio function
- Embedded USB audio applications
- Multi-channel output audio sound card and audio box
- True 7.1 channel output gaming headphone

3.1. System Configuration

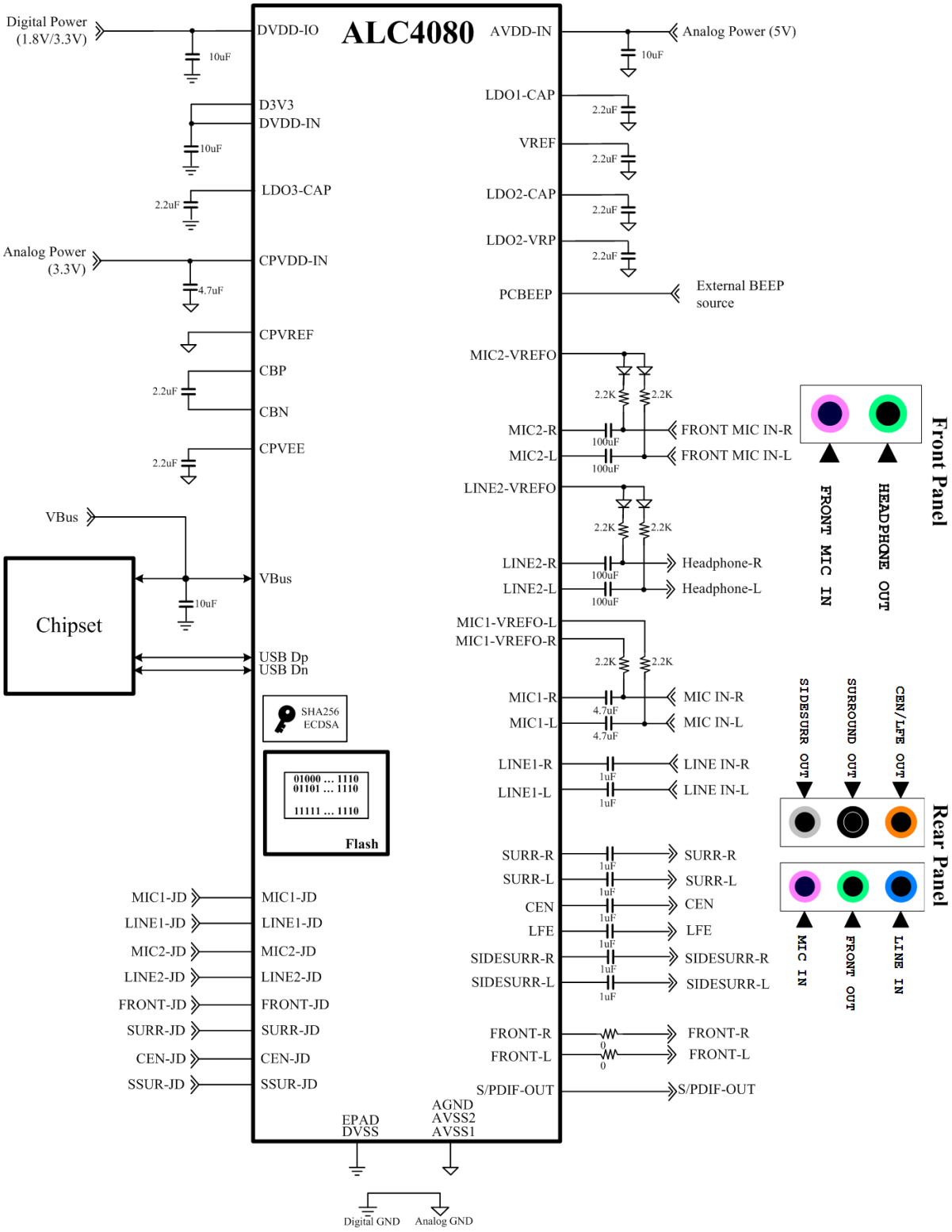


Figure 1. System Configuration

4. Block Diagrams

4.1. Block Diagram – Audio Block

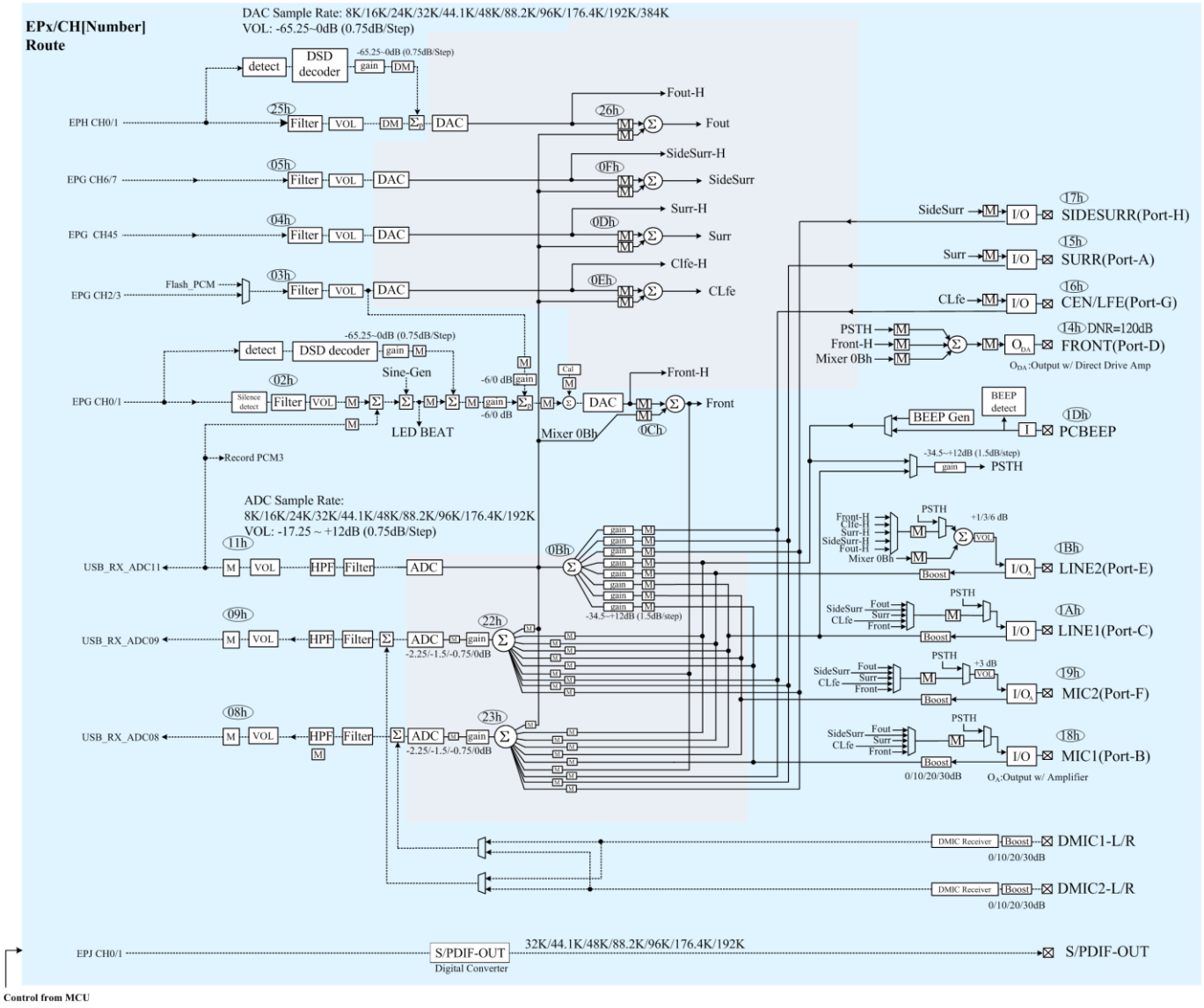


Figure 2. Block Diagram – Audio Block

4.2. Block Diagram – USB Controller

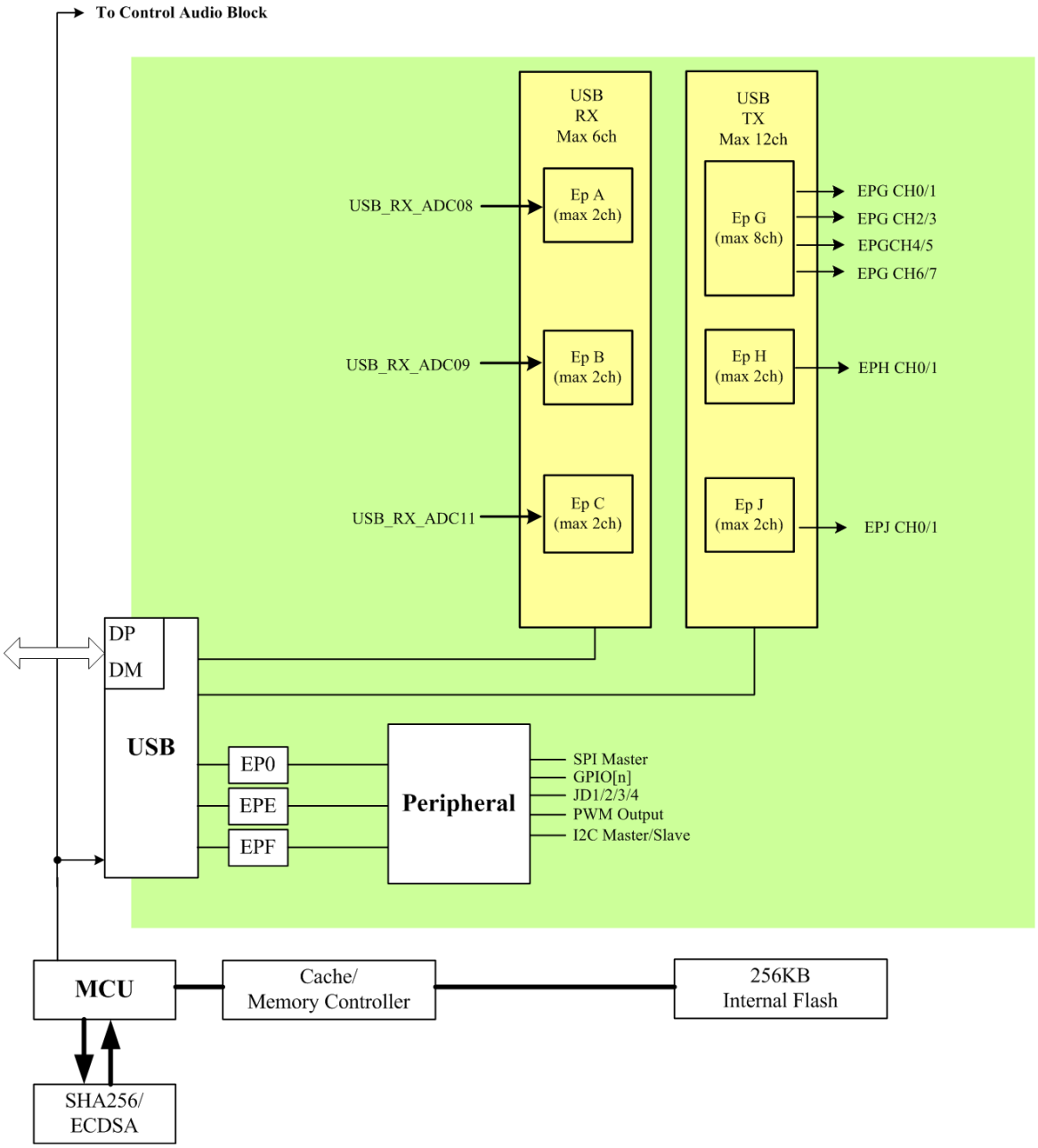


Figure 3. Block Diagram – USB Controller

4.3. Analog Connector and Device

MIC1, MIC2, LINE1, LINE2, CEN/LFE, SURR, and SIDESURR are re-tasking IOs.

MIC2 and LINE2 are embedded Headphone Amplifiers.

FRONT is Capless type output and does not support audio analog input.

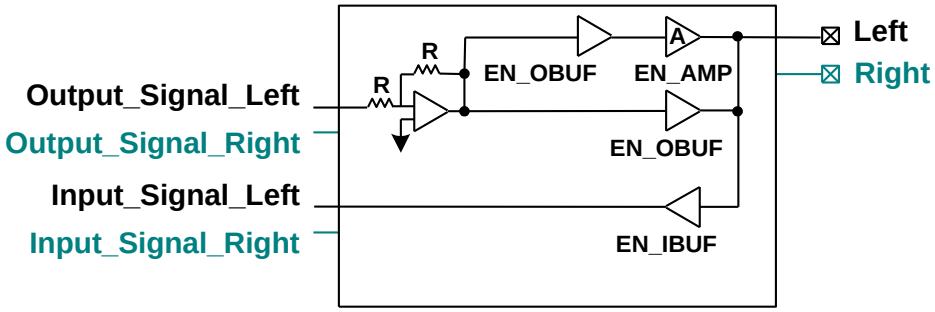


Figure 4. Analog Input/Output Unit

4.4. Jack Detection Resistor Matrix

Table 1. Jack Detection Resistor Matrix

JD1	
R0(100K)	
FRONT-JD R1(200K)	SURR-JD R2(100K)
JD2	
R0(100K)	
MIC1-JD R1(200K)	CLFE-JD R2(100K)
JD3	
R0(100K)	
MIC2-JD R1(200K)	LINE2-JD R2(100K)
JD4	
R0(100K)	
LINE1-JD R1(200K)	SSURR-JD R2(100K)

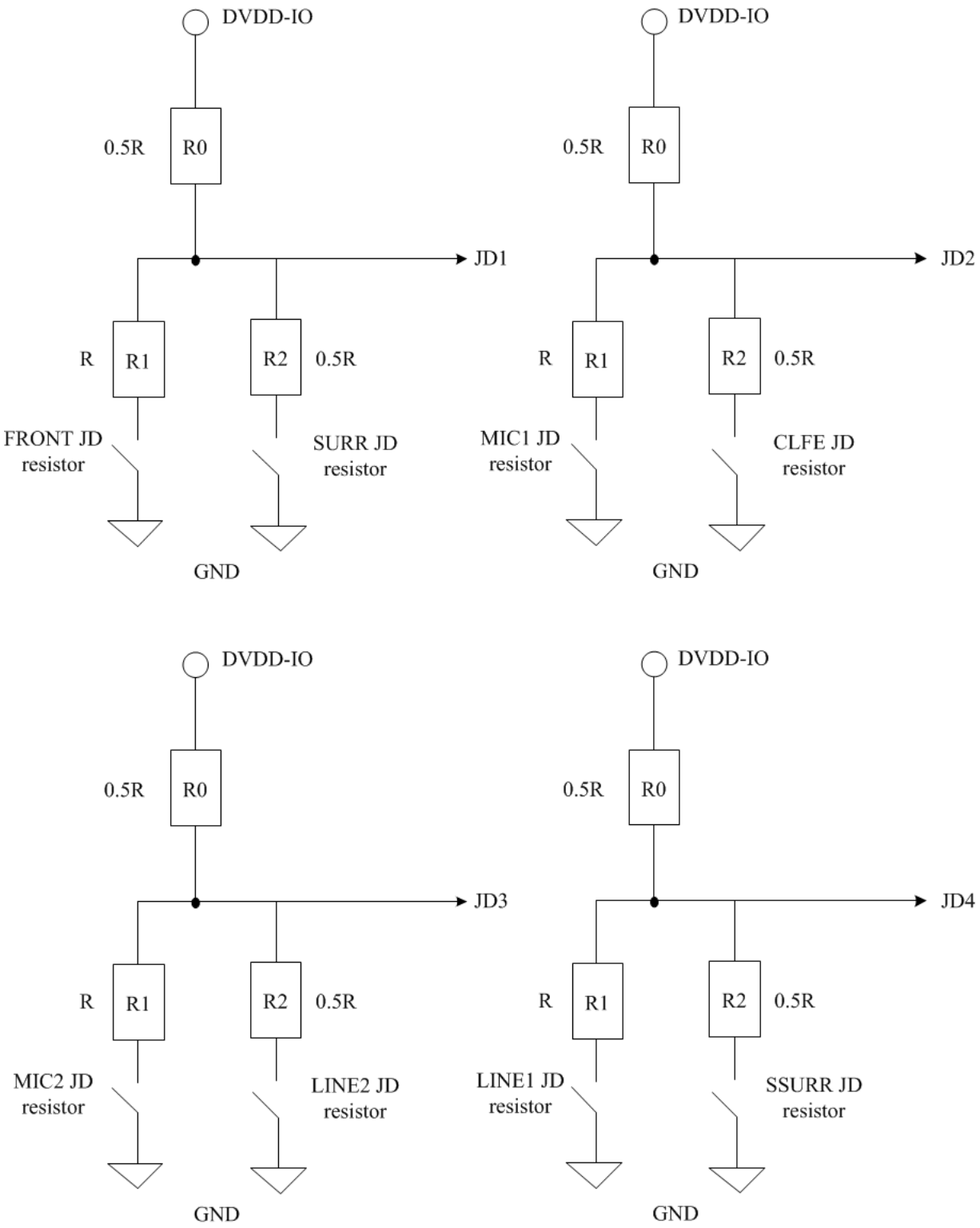


Figure 5. Jack Detection Connection Examples

5. Pin Assignments

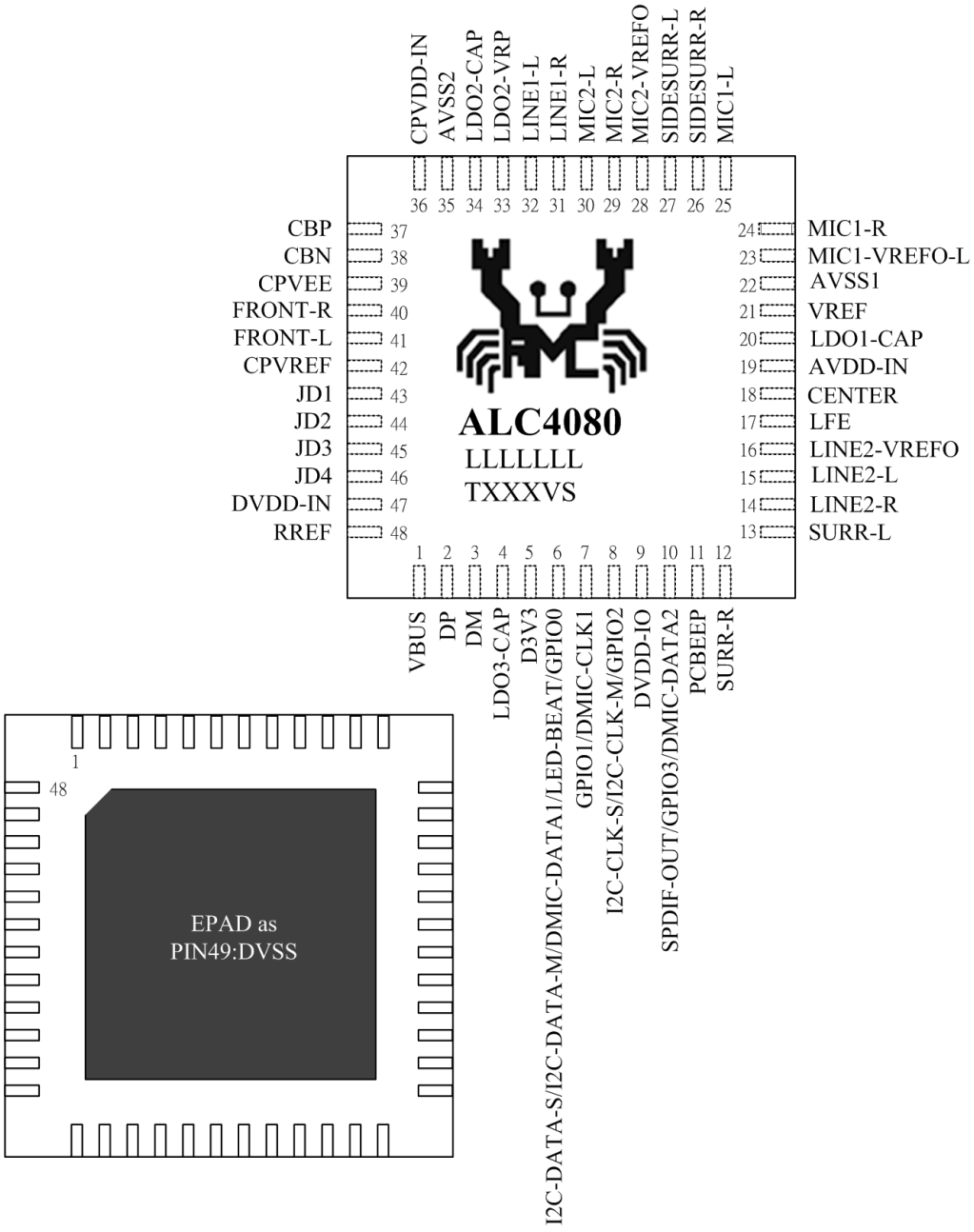


Figure 6. Pin Assignments

5.1. Package and Version Identification

Green package is indicated by a ‘G’ in the location marked ‘T’. The silicon version and step numbers are shown in the location marked ‘V’ and ‘S’.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 2. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
I2C-DATA-S/ I2C-DATA-M/ GPIO0/ DMIC-DATA1/ LED-BEAT	IO	6	I2C slave interface data/ I2C master interface data/ General Purpose Input/Output 0/ Data input from primary digital microphone/ LED drive	Schmitt trigger input, V_{IL}=0.4*DVDD-IO, V_{IH}=0.6*DVDD-IO Output, V_{OL}=0.1*DVDD-IO, V_{OH}=0.9*DVDD-IO
GPIO1/ DMIC-CLK1	IO	7	General Purpose Input/Output 1/ Clock output to primary digital microphone	Schmitt trigger input, V_{IL}=0.4*DVDD-IO, V_{IH}=0.6*DVDD-IO Output, V_{OL}=0.1*DVDD-IO, V_{OH}=0.9*DVDD-IO
I2C-CLK-S/ I2C-CLK-M/ GPIO2	IO	8	I2C slave interface clock/ I2C master interface clock/ General Purpose Input/Output 2	Schmitt trigger input, V_{IL}=0.4*DVDD-IO, V_{IH}=0.6*DVDD-IO Output, V_{OL}=0.1*DVDD-IO, V_{OH}=0.9*DVDD-IO
SPDIF-OUT / GPIO3 / DMIC-DATA2	IO	10	SPDIF output/ General Purpose Input/Output 3/ Data input from secondary digital microphone	Schmitt trigger input, V_{IL}=0.4*DVDD-IO, V_{IH}=0.6*DVDD-IO Output, V_{OL}=0.1*DVDD-IO, V_{OH}=0.9*DVDD-IO SPDIF output: 12mA@75Ω driving capability.
JD1	I	43	Jack Detect for FRONT and SURR port	Internal pull high/low/float programmable PIN. 3 thresholds to detect 4 states 2.2V/1.65V/1.32V(DVDD-IO=3.3V) (Option for 1 pin detects 1 port)
JD2	I	44	Jack Detect for MIC1 and CEN port	Internal pull high/low/float programmable PIN. 3 thresholds to detect 4 states 2.2V/1.65V/1.32V(DVDD-IO=3.3V) (Option for 1 pin detects 1 port)
JD3	I	45	Jack Detect for MIC2 and LINE2 port	Internal pull high/low/float programmable PIN. 3 thresholds to detect 4 states 2.2V/1.65V/1.32V(DVDD-IO=3.3V) (Option for 1 pin detects 1 port)
JD4	I	46	Jack Detect for LINE1 and SSURR port	Internal pull high/low/float programmable PIN. 3 thresholds to detect 4 states 2.2V/1.65V/1.32V(DVDD-IO=3.3V) (Option for 1 pin detects 1 port)
				Total: 8 Pins

Note1: PWM output can be configured from the PWM1/PWM2/PWM3 unit.

6.2. Analog I/O Pins

Table 3. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
PCBEEP	I	11	External PC Beep Input	Analog Input: 1.5Vrms of full-scale input
SURR-R	IO	12	Analog Input and Output (Right)	Analog I/O (PORT-A-R), default surround channel
SURR-L	IO	13	Analog Input and Output (Left)	Analog I/O (PORT-A-L), default surround channel
LINE2-R	IO	14	Analog Input and Output with Multiple Function (Right)	Analog I/O (PORT-E-R), default 2nd line input. Recommended to be re-tasking port at front panel
LINE2-L	IO	15	Analog Input and Output with Multiple Function (Left)	Analog I/O (PORT-E-L), default 2nd line input. Recommended to be re-tasking port at front panel
LFE	IO	17	Analog Input and Output (Right)	Analog I/O (PORT-G-R), default LFE channel
CENTER	IO	18	Analog Input and Output (Left)	Analog I/O (PORT-G-L), default center channel
MIC1-R	IO	24	Analog Input and Output with Multiple Function (Right)	Analog I/O (PORT-B-R), default 1st microphone input. Recommended to be microphone input at rear panel
MIC1-L	IO	25	Analog Input and Output with Multiple Function (Left)	Analog I/O (PORT-B-L), default 1st microphone input. Recommended to be microphone input at rear panel
SIDESURR-R	IO	26	Analog Input and Output (Right)	Analog I/O (PORT-H-R), default side surround channel
SIDESURR-L	IO	27	Analog Input and Output (Left)	Analog I/O (PORT-H-L), default side surround channel
MIC2-R	IO	29	Analog Input and Output with Multiple Function (Right)	Analog I/O (PORT-F-R), default 2nd microphone input. Recommended to be re-tasking port at front panel
MIC2-L	IO	30	Analog Input and Output with Multiple Function (Left)	Analog I/O (PORT-F-L), default 2nd microphone input. Recommended to be re-tasking port at front panel
LINE1-R	IO	31	Analog Input and Output with Multiple Function (Right)	Analog I/O (PORT-C-R), default 1st line input. Recommended to be line level input at rear panel
LINE1-L	IO	32	Analog Input and Output with Multiple Function (Left)	Analog I/O (PORT-C-L), default 1st line input. Recommended to be line level input at rear panel
FRONT-R	IO	40	Analog Input and Output (Right)	Analog I/O (PORT-D-R), default front channel
FRONT-L	IO	41	Analog Input and Output (Left)	Analog I/O (PORT-D-L), default front channel
				Total: 17 Pins

6.3. Filter/Reference Pins

Table 4. Filter/Reference Pins

Name	Type	Pin	Description	Characteristic Definition
LDO3-CAP	-	4	Internal LDO supplied to digital core power	4.7µF capacitor to **digital** ground
D3V3	-	5	Digital power generated internally	2.2µF capacitor to **digital** ground
LINE2-VREFO	O	16	Bias Voltage for LINE2	2.25V/3.2V/4.0V reference voltage
LDO1-CAP	-	20	Internal LDO supplied to analog IO power	10µF capacitor to **analog** ground
VREF	-	21	2.25V Reference Voltage	10µF capacitor to **analog** ground
MIC1-VREFO-L	O	23	Bias Voltage for MIC1-L	2.25V/3.2V/4.0V reference voltage
MIC2-VREFO	O	28	Bias Voltage for MIC2	2.25V/3.2V/4.0V reference voltage
LDO2-VRP	-	33	LDO2 Reference Voltage	100µF capacitor to **analog** ground
LDO2-CAP	-	34	Internal LDO supplied to analog core power	10µF capacitor to **analog** ground
CBP	-	37	Charge pump Bucket Capacitor	2.2µF capacitor to CBN
CBN	-	38	Charge pump Bucket Capacitor	2.2µF capacitor to CBP
CPVEE	-	39	Reference Voltage Output	2.2µF capacitor to **analog** ground
CPVREF	-	42	Ground Reference for charge pump	Connected to **analog** ground
				Total: 13 Pins

6.4. Power & Ground Pins

Table 5. Power & Ground Pins

Name	Type	Pin	Description	Characteristic Definition
DVDD-IO	P	9	Digital power input for jack detection and digital IO apart from SPI	Digital VDD (1.8V/3.3V)
AVDD-IN	P	19	Analog power input for analog circuit	Analog VDD (5V)
AVSS1	G	22	Analog ground for Mixer and IO	Analog GND
AVSS2	G	35	Analog ground for DAC and ADC	Analog GND
CPVDD-IN	P	36	Power input for charge pump	Digital VDD (3.3V)
DVDD-IN	P	47	Digital power input for digital circuit Typically connected to D3V3.	Digital VDD (3.3V)
VBUS	P	1	USB bus 5.0V power input for integrated multiple regulators. It also accepts 3.3V of power input for 3.3V USB system	USB Bus power for whole chip (3.3V/5V)
EPAD	G	49	Ground for digital circuit	Digital ground
				Total: 8 Pins

6.5. USB Transceiver Interface

Table 6. USB Transceiver Interface Pins

Name	Type	Pin	Description	Characteristic Definition
DP	IO	2	USB D+ signal	Current mode and connected to USB Host
DM	IO	3	USB D- signal	Current mode and connected to USB Host
RREF	-	48	Reference bias for USB current source	Connected to resistor to ground (Requires 1% precision 6.25k or 6.2k)
				Total: 3 Pins

7. Electrical Characteristics

7.1. DC Characteristics

7.1.1. Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies Digital Power	 VBUS DVDD-IO DVDD-IN CPVDD-IN AVDD-IN	 -0.3 -0.3 -0.3 -0.3 -0.3	 5 3.3 3.3 3.3 5	 5.5 3.63 3.63 3.63 5.5	 V V V V V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-40	-	+125	°C
ESD (Electrostatic Discharge) Susceptibility Voltage					
All Pins	Pass 3500V				

7.1.2. Recommended Operating Conditions

Table 8. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies: Digital Power	 VBUS DVDD-IO DVDD-IN CPVDD-IN AVDD-IN	 3.0 1.71 3.0 3.0 4.5	 3.3 / 5 1.8 / 3.3 3.3 3.3 5	 5.5 3.63 3.63 3.63 5.5	 V V V V V

7.1.3. Threshold Voltage

DVDD-IO=1.8V/3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 9. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD-IO+0.30	V
Low Level Input Voltage (SPDIF-OUT, DMIC-DATA, GPIOs)	V_{IL}	-	0.4* DVDD-IO	-	V
High Level Input Voltage (SPDIF-OUT, DMIC-DATA, GPIOs)	V_{IH}	-	0.6* DVDD-IO	-	V
Low Level Output Voltage (SPDIF-OUT, DMIC-CLK, GPIOs)	V_{OL}	-	-	0.1* DVDD-IO	V
High Level Output Voltage (SPDIF-OUT, DMIC-CLK, GPIOs)	V_{OH}	0.9* DVDD-IO	-	-	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	4	-	mA
Internal Pull Up/Down Resistance	-	-	200k	-	Ω

7.1.4. SPDIF Output Characteristics

DVDD-IO= 3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 10. SPDIF Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
SPDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
SPDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V

7.2. Digital & Analog Filter Characteristics

Table 11. Digital & Analog Filter Characteristics

Filter	Symbol		Minimum	Typical	Maximum	Units
ADC	Frequency response	FS=48K(20~20KHz) FS=96K(20~40KHz)	-0.405 -2.411	- -	-0.015 0.019	dB
	Stopband		0.6*Fs	-	-	kHz
	Stopband Rejection		-	-90	-	dB
DAC	Frequency response	FS=48K(20~20KHz) FS=96K(20~40KHz)	-0.058 -0.107	- -	0.003 0.001	dB
	Stopband		0.5465*Fs	-	-	kHz
	Stopband Rejection		-	-105	-	dB

Note: Fs=Sample rate.

7.3. AC Characteristics

7.3.1. I2C Control Interface

Table 12. I2C Control Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Clock Low Pulse Duration	Tw(9)	1.3	-	-	µs
Clock High Pulse Duration	Tw(10)	0.6	-	-	µs
Clock Frequency	f	0	-	400	KHz
Setup Time for a Repeated START Condition	Tsu(6)	600	-	-	ns
Start Hold Time	Th(5)	600	-	-	ns
Data Setup Time	Tsu(7)	100	-	-	ns
Data Hold Time	Th(6)	-	-	900	ns
Rising Time	Tr	-	-	300	ns
Falling Time	Tf	-	-	300	ns
Setup Time	Tsu(8)	600	-	-	ns
Bus Free Time Between a STOP and START Condition	Tbuf	1.3	-	-	µs
Pulse Width of Spikes Suppressed Input Filter	Tsp	0	-	50	ns

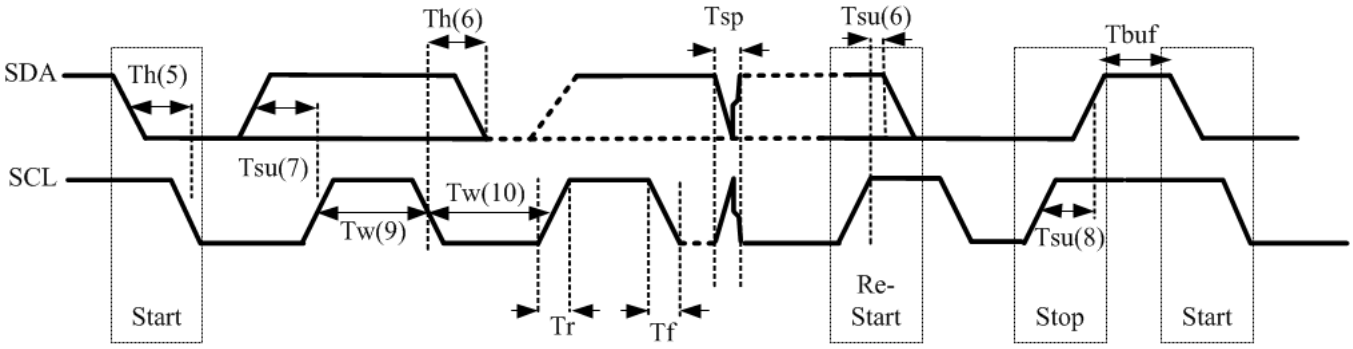


Figure 7. I2C Control Interface Timing Diagram

7.3.2. SPDIF Output Interface

Table 13. SPDIF Output Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
SPDIF-OUT Frequency	-	-	3.072	-	MHz
SPDIF-OUT Period *1	T_{cycle}	-	325.6	-	ns
SPDIF-OUT Jitter	T_{jitter}	-	-	4	ns
SPDIF-OUT High Level Width	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Low Level Width	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
SPDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns

**1: Bit parameters for 48kHz sample rate of SPDIF-OUT.*

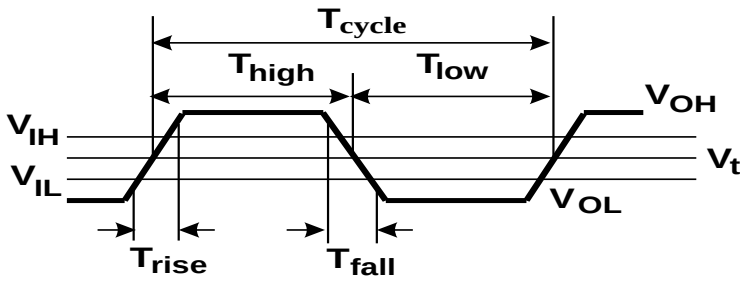


Figure 8. SPDIF Output Timing Diagram

7.4. Analog Performance

Standard Test Conditions

- $T_{ambient}$=25ºC, AVDD-IN=5.0V±5%, CPVDD-IN=3.3V±5%
- 997Hz input Full Scale sine wave; Sampling frequency=48kHz
- Test bench Characterization BW: 20Hz~22kHz
- 10KΩ/100pF load for Line Out
- 16Ω/100pF, 32Ω/100pF, 150Ω/100pF, 10KΩ/100pF load for Headphone Out
- All volume gain set to 0dB

Table 14. Analog Performance

Parameter	Min	Typical	Max	Units
Full-Scale Input Voltage				
ADC09h from MIC2	-	1.9	-	Vrms
ADC09h from LINE1	-	1.9	-	Vrms
ADC09h form except MIC2/LINE1	-	1.5	-	Vrms
ADC08h/11h from Input	-	1.3	-	Vrms
Full-Scale Output Voltage (Gain=0dB)				
FRONT DAC02h to Output 14h @16Ω Load	-	0.8	-	Vrms
@32Ω Load	-	1.5	-	Vrms
@150Ω Load	-	2.1	-	Vrms
@10KΩ Load	-	2.2	-	Vrms
FRONT DAC02h to except Output 14h	-	1.1	-	Vrms
All DAC to Output 1Bh	-	1.2	-	Vrms
Other DAC to Output	-	1.1	-	Vrms
Dynamic Range with –60dB Signal (A-Weight)				
FRONT DAC02h to Output 14h @16Ω Load	-	115	-	dB FSA
@32Ω Load	-	118	-	dB FSA
@150Ω Load	-	120	-	dB FSA
@10KΩ Load	-	120	-	dB FSA
FRONT DAC02h to except Output 14h	-	98	-	dB FSA
FRONT DAC02h to Output 1Bh	-	110	-	dB FSA
Other DACs	-	98	-	dB FSA
Dynamic Range with –60dB Signal (A-Weight)				
ADC09h from MIC2	-	110	-	dB FSA
ADC09h from LINE1	-	110	-	dB FSA
ADC09h from except MIC2/LINE1	-	98	-	dB FSA
Other ADCs	-	92	-	dB FSA
THD+N with –3dB Signal (No A-Weight)				
ADC	-	-87	-	dB FS
DAC	-	-89	-	dB FS
DAC to Headphone Amplifier Output @16Ω Load	-	-85	-	dB FS
@32Ω Load	-	-87	-	dB FS
@150Ω Load	-	-90	-	dB FS
@10KΩ Load	-	-90	-	dB FS

Parameter	Min	Typical	Max	Units
Magnitude Response (10KΩ Load)				
All DAC @Fs=48KHz (FR=±0.05dB)	0	-	21,792	Hz
All DAC @Fs=96KHz (FR=±0.05dB)	0	-	43,584	Hz
All DAC @Fs=192KHz (FR=±0.05dB)	0	-	87,168	Hz
All ADC @Fs=48KHz (FR=±0.04dB)	0	-	19,200	Hz
All ADC @Fs=96KHz (FR=±0.04dB)	0	-	38,400	Hz
All ADC @Fs=192KHz (FR=±0.04dB)	0	-	76,800	Hz
Power Supply Rejection Ratio(Measure at 1KHz Point)	-	-60	-	dB
Amplifier Gain Step				
ADC	-	0.75	-	dB
DAC	-	0.75	-	dB
Crosstalk (10K loading)	-	-80	-	dB
Input Impedance (Gain=0dB)				
LINE1 (High Performance)	-	45	-	KΩ
LINE1 (Normal)	-	32	-	KΩ
Others	-	64	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-Amplified Output	-	100	-	Ω
VREFOUTx Output Voltage	2.25	3.2	4.0	V
VREFOUTx Output Current	-	5	-	mA
Power consumption @ Active Mode (*2)	-	TBD	-	mW
Power consumption @ Idle support UAC1 and HID class	-	TBD	-	mW
Power consumption @ Idle support HID class	-	TBD	-	mW
Power consumption @ suspend	-	TBD	-	μW

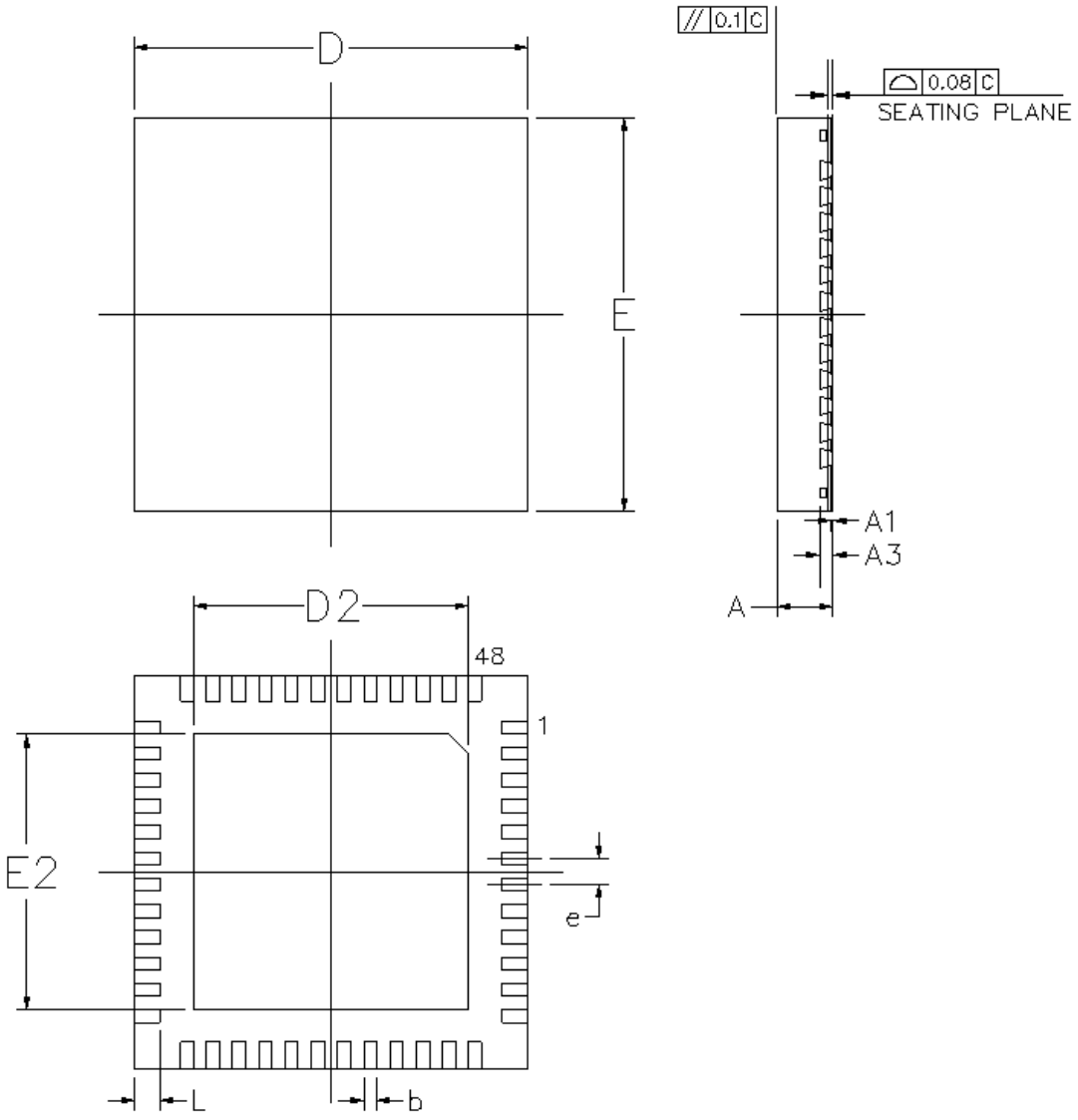
Note 1: FSA=Full-Scale with A-weighting filter. *FS=Full-Scale.*
Note 2: Only DAC to Headphone out @32ohm 1mW output power.
Note 3: THDN is 1% at least defined to full scale output voltage.

8. Application Circuits

Please contact Realtek for up-to-date application circuit information.

9. Mechanical Dimensions

9.1. Mechanical Dimensions – QFN 48 6x6 Outline



9.2. Mechanical Dimension Notes

Table 15. Dimensions Table

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D_2/E_2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER (mm).*
2. *REFERENCE DOCUMENT: JEDEC MO-220.*

10. Ordering Information

Table 16. Ordering Information

Part Number	Package	Status
ALC4080-VA2-CG	QFN-48 (6mm x 6mm) 'Green' Package	ES

Note: See page 11 for Green package and version identification.

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